



AD8302-based polar demodulator interface for impedance spectroscopy oriented to biomedical applications

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ABSTRACT

This paper proposes a polar demodulator circuit architecture for electrical impedance spectroscopy. The proposed system implements a dynamic gain inverting amplifier and a signal network conditioning technique to effectively utilize the AD8302 RF/IF gain and phase detector across a wide frequency range. The implemented feedback gain control allows the integrated circuit to expand the measurable impedance range while maintaining high linearity of response from 100 Hz to over 10 MHz exhibiting the maximum modulus and phase errors of 14.42% and 5.73°, respectively. This performance represents an advancement over existing impedance measurement systems that implements commercial ICs, particularly in applications where wide-range, high-accuracy measurements are critical. The architecture enable a multifrequency electrical bioimpedance spectroscopy across a broad frequency spectrum where low and high-frequency information provide valuable analytical insights.

1. Introduction

Impedance spectroscopy emerges as a sophisticated analytical methodology for comprehensively investigating the electrical properties of materials across an extensive frequency spectrum. Building on this approach, electrical impedance spectroscopy has become a cutting-edge method for analyzing cellular biological activities both quantitatively and qualitatively. This technique provides significant benefits, such as detection without labeling requirements, non-destructive sample analysis, and continuous real-time monitoring [1,2]. Impedance-based sensors find primary use in electroanalysis and biosensing by detecting minute impedance changes at electrode–electrolyte interfaces to identify specific analytes. In biomedical applications, they enable valuable non-invasive analysis of cells, tissues, and biological systems. Their compact size and low cost also make them suitable for wearable health monitoring applications [3].

Measurement requirements vary widely depending on the application. For instance, pulmonary imaging [4] and ECG monitoring [5] typically require frequencies up to 200 kHz, while more demanding applications—such as prostate cancer monitoring [6], cellular analysis [7], blood characterization [8], breast cancer diagnostics [9], and hepatic imaging [10]—benefit from measurements extending to 1 MHz or beyond. These high-frequency applications pose significant design challenges, as impedance measurement circuits become increasingly

sensitive to non-ideal delays and errors, leading to higher energy consumption and potential limitations in wearable device autonomy.

To tackle these measurement challenges, different impedance-measurement circuit architectures have been developed. Typical approaches include In-phase and Quadrature (I/Q) demodulation, digital demodulation, and polar demodulation. I/Q architectures extract the real and imaginary components of the impedance by mixing the output of an instrumentation amplifier (IA) with in-phase and quadrature versions of the excitation signal, making them suitable for narrowband measurements but limited at high frequencies by IA bandwidth and phase-shifting requirements [11,12]. Digital demodulation performs the extraction numerically after high-speed sampling, offering flexibility but increasing power consumption [13,14]. Polar demodulation directly measures modulus and phase via a reference path, improving robustness to delay and nonlinearity, although XOR-based phase detection may introduce errors at high frequencies [15–17]. Each approach involves trade-offs in bandwidth, accuracy, complexity, and power consumption, and their selection depends on the specific application requirements.

Traditionally, impedance spectroscopy systems comprise a signal generator and an impedance measurement circuit. The generator applies an excitation signal, typically a current stimulus, to the system under investigation, while the measurement circuit extracts impedance

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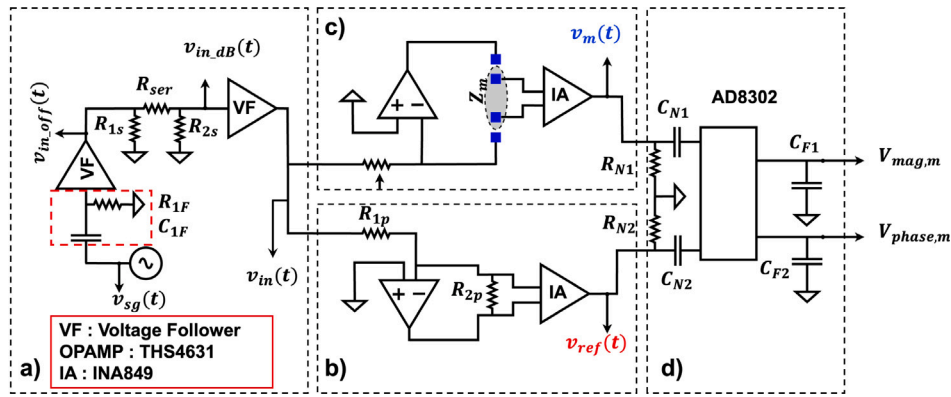


Fig. 1. Simplified block diagram presenting the architecture of the proposed impedance-measurement circuit.

information by detecting voltage or comparing against a reference signal. Data acquisition can follow either broadband excitation or single-frequency progressive scanning; in this work, we focus on frequency-sweep architectures.

Recent research has emphasized the development of precise, broadband impedance measurement systems, both through custom-designed integrated circuits (ICs) and via commercial components such as the AD5933 [18–20], AD9850 [21,22], and AD8302 [23–26] with specialized interfacing. Among these ICs, impedance characterization is typically limited to 100 kHz due to the slew-rate and bandwidth constraints of the operational amplifiers.

To overcome these limitations, we present an architecture based on the AD8302, enabling impedance measurements up to 10 MHz with excellent precision. The proposed design includes an analog front-end with high-slew-rate operational amplifiers, a high-bandwidth IA, and a feedback gain control to optimize performance across lower frequency ranges. The AD8302 comprises a matched pair of demodulating logarithmic amplifiers, each with a 60 dB measurement range; the difference of their outputs provides a measurement of the modulus ratio. A multiplier-type phase detector ensures precise phase balance, driven by the fully limited signals from the logarithmic amplifiers' outputs.

2. Material and methods

2.1. Overall architecture

Fig. 1 shows a schematic diagram of the proposed polar demodulator. A signal generator is used to provide the input signal for the measurement of the unknown impedance, Z_m . As reported in Fig. 1(a), before being applied to the measurement circuit, the input signal, $v_{in}(t)$, is first conditioned through a first-order high-pass filter (HPF), implemented as a CR ($R_{1F} = 1 \text{ M}\Omega$ and $C_{1F} = 1 \text{ }\mu\text{F}$) network followed by a voltage follower (VF), with a cut-off frequency of 0.16 Hz in order to remove the DC offset from the input signal, $v_{in}(t)$. After this stage an attenuation network of -16 dB (R_{1s} and $R_{2s} = 68 \text{ }\Omega$; $R_{ser} = 150 \text{ }\Omega$) is implemented to the input signal before the inverting stage.

For the analysis of Z_m , a 100 mV peak-to-peak signal is applied to two paths: a reference stage with fixed gain $G_p \approx R_{2p}/R_{1p} \approx 4.7$ (where $R_{2p} = 4.7 \text{ k}\Omega$ and $R_{1p} = 1 \text{ k}\Omega$) and the measurement stage.

The reference stage is designed to compensate for the 90° phase shift introduced by the op-amp configuration and to synchronize the two signals.

The measurement stage employs an inverting configuration using a wideband FET-input op-amp (THS4631) in a dynamic gain configuration, implemented with a resistor bank controlled by two multiplexers. This ensures a gain ratio below $+20 \text{ dB}$, thereby guaranteeing the maximum achievable bandwidth (GBW) of the amplifier for the selected configuration.

Two ultra-low-noise instrumentation amplifiers (INA849) with 0 dB gain amplify $v_{ref}(t)$ along the reference path and $v_m(t)$ along the measurement path. This setup decouples the current path from the voltage measurement path, allowing both 2-electrode and 4-electrode configurations.

Once the signal has been extracted from the instrumentation amplifier (IA), is applied to the input of the AD8302. The AD8302 is a commercial IC, originally designed for RF/IF gain and phase detection up to 1 GHz. The IC exhibits a mean sensitivity of 30 mV/dB for the modulus and 10 mV/degree for the phase. Since the linearity range is approximately $\pm 30 \text{ dB}$ for the modulus and between 0 and 180° for the phase, the bank of resistor is dimensioned in order to maintain a ratio less than $+20 \text{ dB}$ for the impedance range from 100-1 M Ω . In order to use this IC at low frequency the input stage network is dimensioned to impedance matching (R_{N1} and $R_{N1} = 50 \text{ }\Omega$) and move the nominal high-pass corner frequency, f_{HP} , of this loop that is set internally at 200 MHz but it is lowered by adding external capacitance to the input stage network. In this case, external capacitances C_{N1} and C_{N2} , each equal to 100 μF , are added to set the high-pass corner frequency, f_{HP} , at 31 Hz.

In the IC, each log amp consists of a cascade of six 10 dB gain stages with seven associated detectors. The individual gain stages have 3 dB bandwidths in excess of 5 GHz. The signal path is fully differential to minimize the effect of common-mode signals and noise. Since there is a total of 60 dB of cascaded gain, slight dc offsets can cause limiting of the latter stages, which may cause measurement errors for small signals. In order to test the architecture, the designed circuit is implemented in a 4-layer PCB with thermal dissipation with a dual-supply of $\pm 5 \text{ V}$. The analog front-end incorporates a signal conditioning architecture for DC offset elimination the input signal, followed by an attenuation stage of 16 dB. The low-impedance signal is then distributed across two critical signal paths: a fixed-gain inverting operational amplifier configuration generating a reference signal as reported in Fig. 1(b), while a dynamic operational amplifier configuration adapts to the unknown impedance under test, Fig. 1(c). The processed signals are subsequently applied to the input of INA849 high-bandwidth, ultra-low noise instrumentation amplifier, to ensure signal integrity and decouple the current path to the measured voltage path. In the final stage, the conditioned reference and test signals are simultaneously applied to the AD8302, Fig. 1(d), for comprehensive signal analysis.

2.2. Dynamic gain inverting amplifier

The fundamental logic behind the dynamic gain control of the inverting amplifier focuses on precisely managing the ratio between the reference resistance R_{ser} and Z_m across the entire frequency spectrum, an approach already used in one of our previous works [17]. This strategic approach aims to maintain the circuit's operation within the linear range while simultaneously expanding the measurable impedance

spectrum. By dynamically adapting the gain, the circuit can mitigate significant performance limitations that arise from substantial impedance mismatches. Substantial differences between R_{set} and Z_m can lead to bandwidth reduction, resulting in signal attenuation and consequent estimation errors of the device's impedance characteristics. To address these challenges, a feedback gain control mechanism is implemented through a dynamically configurable resistance bank. This bank is selectively switched via a multiplexer, which is controlled by a microcontroller (μC). The μC 's primary function is to optimize R_{set} selection for the unknown impedance, while maintaining a critical constraint of keeping the ratio between reference voltage $v_{ref}(t)$ and measurement voltage $v_z(t)$ below 20 dB while sampling the signal an analog-to-digital converter (ADS1115). By continuously monitoring the ratio variations between these two signals, the system can adaptively and opportunistically select the most appropriate R_{set} to ensure optimal measurement accuracy and linearity across varying impedance conditions.

The AD8302 takes the difference in the output of two identical log amps, each driven by signals of similar waveforms but at different levels. Since subtraction in the logarithmic domain corresponds to a ratio in the linear domain, the resulting output becomes:

$$V_{MAG} = V_{SLP}(V_{INA}/V_{INB}) \quad (1)$$

$$mag(\text{dB}) = \log_{10} \left(\frac{V_{INPA}}{V_{INPB}} \right) = \frac{V_{MAG} - V_{0\text{dB}}}{30 \text{ mV}} \quad (2)$$

where V_{INA} and V_{INB} are the input voltages, V_{MAG} is the output corresponding to the modulus of the signal level difference, and V_{SLP} is the slope of 30 mV/dB.

The log amplifier architecture comprises cascaded linear and limiting gain stages with demodulating detectors. The output of the final stage in each log amp is a fully amplitude-limited sinusoidal signal over the majority of the input dynamic range, preserving phase information. These conditioned signals are subsequently applied to an analog vector (multiplicative) phase detector, which performs a continuous-time multiplication of the two inputs. After low-pass filtering ($C_{F1}, C_{F2} = 10 \mu\text{F}$), the detector generates a DC voltage proportional to the cosine of the phase difference between the inputs, rendering the measured phase independent of input signal amplitudes and providing a linear response over a defined central phase range. The phase output has the general form:

$$V_{PHASE} = V_{\phi}(\phi V_{INA} - \phi V_{INB}) \quad (3)$$

$$\theta(\text{degree}) = [\theta_{INPA} - \theta_{INPB}] = \frac{V_{0^\circ} - V_{PHASE}}{10 \text{ mV}} \quad (4)$$

where V_{ϕ} is the phase slope of 10 mV/degree and ϕ is each signal's relative phase in degrees. To ensure accurate phase estimation across the entire frequency sweep, reference voltages corresponding to 0° phase (V_{0°) were experimentally acquired for each test frequency and used in the calculation.

2.3. Noise analysis

Fig. 2 presents the input-referred noise spectral density, expressed in $\text{nV}/\sqrt{\text{Hz}}$, for the output of the logarithmic amplifier. Integrating the spectra over the 100 Hz–10 MHz band, the resulting $V_{mag,noise}$ and $V_{phase,noise}$ are respectively 1.08 mV and 1.11 mV. These results indicate that thermal noise, flicker noise ($1/f$), and shot noise represent the main limiting factors.

The SNR calculated at the analog front-end preceding the AD8302 reaches a maximum of 31.1 dB, in agreement with expectations for a wideband INA–op-amp stage. Measured SNR varies from 25 to 31 dB across the investigated frequency range, peaking around 1 kHz. The SNR reduction at low frequencies is consistent with flicker noise contributions, while degradation at higher frequencies is primarily due to broadband noise integration.

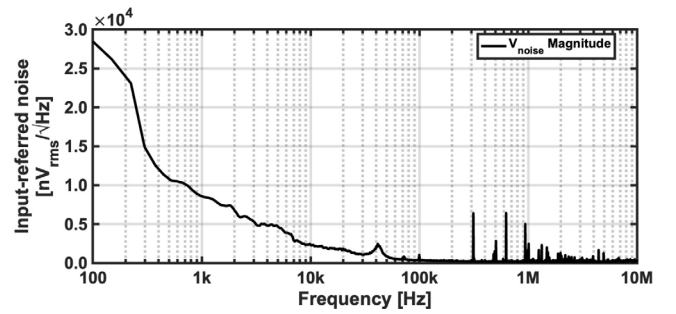


Fig. 2. Input-referred voltage noise spectra for the output $V_{mag,m}$ under nominal operating conditions.

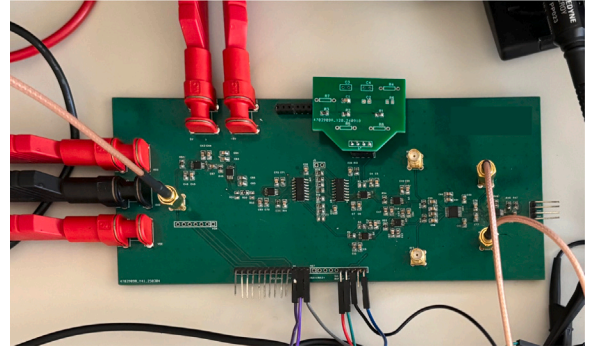


Fig. 3. Picture of the experimental setup featuring the designed PCB implementing the proposed polar demodulation architecture. The setup includes analog front-end circuitry and interfacing points for external signal sources and measurement equipment.

The following AD8302 phase and gain detector exhibits a dynamic range of 58 dB for magnitude and 46.3 dB for phase, enabling accurate measurement of amplitude and phase variations over a wide range. Overall, the observed SNR and dynamic range behavior aligns with the expected performance of a wideband INA–op-amp front-end.

3. Results and discussion

To evaluate the IC performance, experimental bench tests were conducted to assess the estimation accuracy of modulus and phase. A 4-layer PCB was designed, as shown in Fig. 3, and powered with a $\pm 5 \text{ V}$ dual supply. However, the board layout and components are also designed to support a $\pm 12 \text{ V}$ supply, allowing higher output compliance when needed.

The circuit was tested using bench instruments from Teledyne LeCroy, including a T3PS33203P power supply, a T3AFG30 waveform generator, and an HDO6054 bench oscilloscope. The proposed PCB consumes 500 mW of power over the entire frequency range, while output values from the peak detectors and the phase detector were acquired by a microcontroller for further processing and analysis.

The initial validation involved evaluating the electronic interface of the AD8302 through signals with known phase shifts and attenuations in dB, as shown in Fig. 4(a) and in Fig. 4(b). As depicted in Fig. 4(a), the output voltage V_{phase} characteristics were analyzed across a phase shift range of $\pm 180^\circ$, including a detailed measurement error analysis. Complementarily, Fig. 4(b) presents the V_{mag} voltage variation in relation to the decibel attenuation between inspected signals, along with the corresponding error evaluation.

The experimental results corroborate the manufacturer's datasheet specifications, revealing a linear estimation range for modulus between $\pm 20 \text{ dB}$ and a phase measurement error confined within acceptable tolerances.

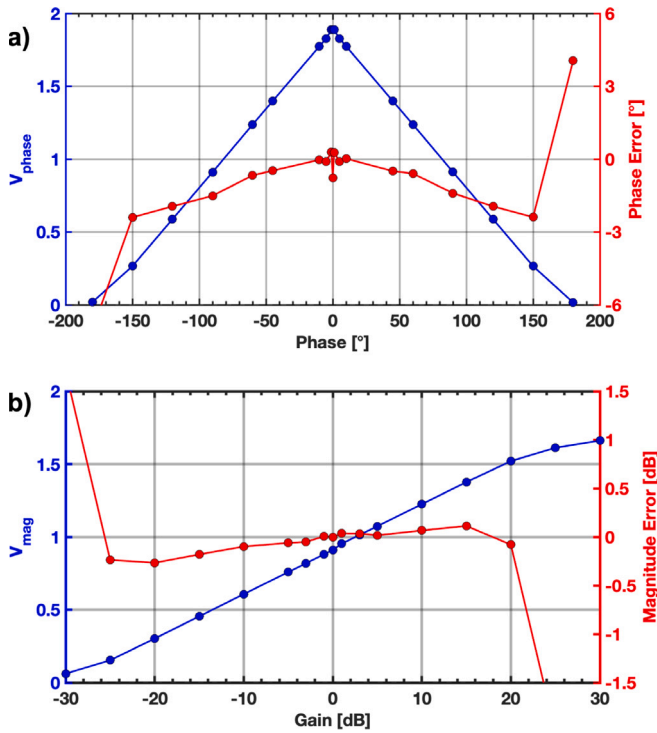


Fig. 4. (a) Phase voltage (V_{phase}) output at various phase shift values (blue dots), with corresponding phase estimation error reported in degrees (red dots); b) modulus voltage (V_{mag}) output across different decibel levels (blue dots), with corresponding modulus estimation error reported in dB (red dots)

The tests conducted involved using a signal generator for the input signal, while an ADC was incorporated into the circuit PCB for reading the output signal. The tests were carried out through three independent experiments, and the standard deviation is reported in Fig. 5. The test impedance, shown in Fig. 5(a), was used to evaluate the electronic interface through a load characterized by a high phase shift and a reduction of the impedance modulus.

A phase calibration was performed at each frequency point to verify the theoretical response of the phase detector and to establish the zero-phase reference voltage, V_{0° , used in subsequent phase calculations. For this calibration, both input channels were driven with sinusoids of identical amplitude and frequency, aligned in phase (i.e., 0° phase difference). The output voltage of the phase detector under these conditions was recorded as V_{0° . This reference value compensates for any offset in the detector and ensures that phase measurements remain accurate across the entire frequency sweep.

Since the electrode–tissue interface can significantly affect bioimpedance measurements – especially when dry electrodes are used – its contribution was also evaluated by inserting an electrode contact model in series with each Z_m [27]. Measurements were therefore repeated both with and without the electrode impedance to quantify its effect on the reconstructed modulus and phase.

The electrode model was derived from the characterization reported in [28], where the electrode–skin interface is described as a series resistance followed by a parallel combination of a charge-transfer resistance and a double-layer capacitance. Accordingly, the electrode impedance used in this work was modeled as

$$Z_{\text{el}}(\omega) = R_s + \left(R_{\text{ct}} \parallel \frac{1}{j\omega C_{\text{dl}}} \right),$$

with

$$R_s = 680 \, \Omega, \quad R_{\text{ct}} = 34 \, \text{k}\Omega, \quad C_{\text{dl}} = 200 \, \text{nF}.$$

Table 1

Performance summary and comparison with state-of-the-art works.

	IC	Frequency range [Hz]	Impedance range [Ω]	Modulus error [%]	Phase error [$^\circ$]
This work	AD8302	100–10M	100–1M	14.42	5.73
[18]	AD5933	1–100k	100–1M	1	1
[19]	AD5933	1–100k	*	*	*
[20]	AD5933	1k–100k	100–1M	*	*
[32]	AD5933	1k–100k	100–1M	3.5	2.8
[21]	AD9850	5–200k	*	10	*
[22]	AD9850	10–100k	*	10	*
[23]	AD8302	10k–100k	*	*	*
[24]	AD8302	100–100k	*	1.5	*
[25]	AD8302	10k–125k	*	10	2
[26]	AD8302	20k–1M	9–5.7k	5.13	0.4
[33]	MAX30009	1k–500k	10–100k	*	*
[34]	AD5941	10k–150k	10–100k	4.3	3
[35]	AD5941	10k–125k	10–100k	10	2
[36]	AFE4300	1k–511k	1–10k	*	*

* Not reported.

These parameters reproduce the typical dispersive behavior and increased low-frequency impedance of non-gelled dry electrodes, and were included to assess their influence on the overall impedance measurement.

To evaluate the performance of the proposed circuit, experimental tests were conducted using multiple discrete model cells, Z_m , as illustrated in Fig. 5, Fig. 6 and Fig. 7. For each model cell, measurements were performed at three frequencies per decade and compared with the theoretical transfer function of the corresponding impedance considering also the contribution of the electrode impedance Z_{el} , with a signal source applied to the input. The measured responses show excellent agreement with the theoretical predictions, confirming the capability of the proposed circuit to perform high-accuracy impedance measurements, capturing both modulus and phase (up to 60°) over a wide frequency range from 100 Hz to 10 MHz.

The first model cell, shown in Fig. 5(a), consisted of a parallel combination of a 6.8 k Ω resistor and a 2 nF capacitor, connected in series with a 330 Ω resistor [29].

Additionally, two further impedance models were considered—a breast cancer cell model [30] and a biceps Cole–Cole impedance model [31]—with their respective results shown in Figs. 6 and 7.

The experimental results obtained with the proposed circuit exhibit remarkable agreement with the theoretical values derived from the Z_m transfer function, both in terms of modulus and phase.

Fig. 5(b–d), Fig. 6(b–d), and Fig. 7(b–d) present the corresponding error analysis of the results shown in Fig. 5(a–c), Fig. 6(a–c), and Fig. 7(a–c). The maximum modulus deviation observed is 14.46%, where the theoretical impedance is approximately 1690 Ω , corresponding to an absolute estimation error of roughly 266.92 Ω . The maximum measured phase error of 5.73 $^\circ$ with the AD8302 is consistent with its specifications, mainly arising from intrinsic nonlinearity and input mismatches. Since the detector exhibits the largest inaccuracies near 0° and $\pm 180^\circ$ (up to 8 $^\circ$), operating outside these critical regions explains the limited error observed. The very low phase deviation further indicates that this error is deterministic, confirming the stability and repeatability of the system.

3.1. Performance comparison with literature

The use of commercial ICs, as reported in the literature, enables impedance spectrum analysis within a limited frequency range of less than 1 MHz. In contrast, this circuit solution employs high-performance components to achieve a broader frequency spectrum, making it suitable for applications from 100 Hz up to 10 MHz. This extended range

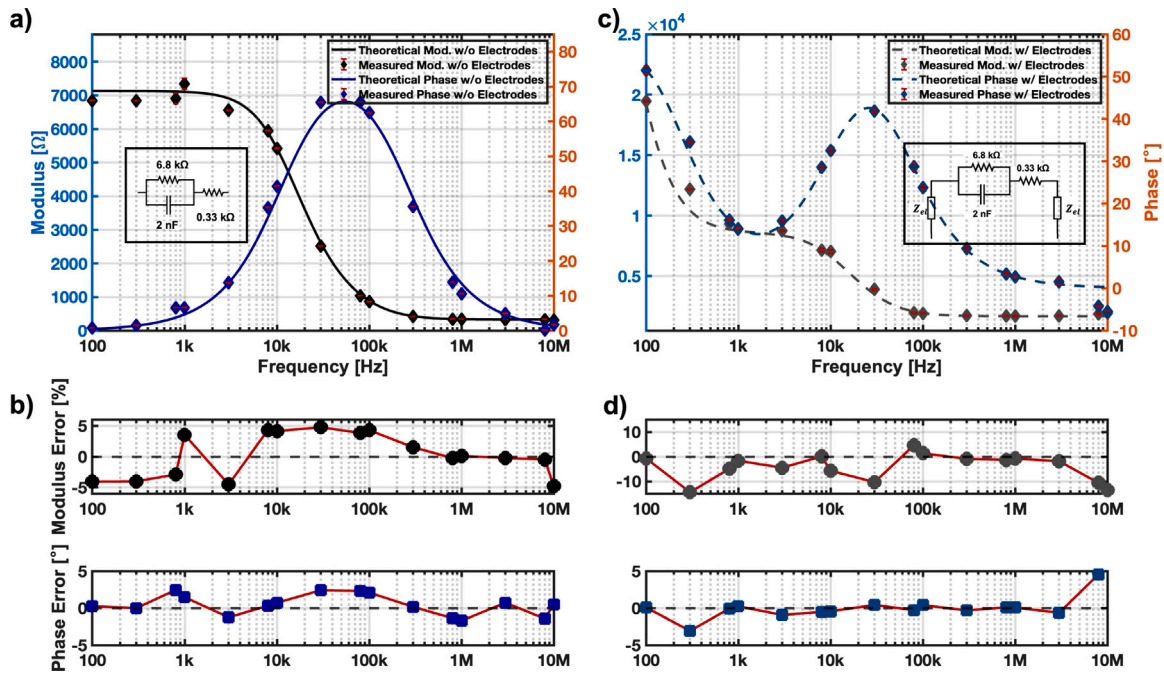


Fig. 5. (a) Experimental and theoretical comparison of impedance modulus and phase for the first model cell over the 100 Hz–10 MHz frequency range. Data are presented as mean \pm SD from three independent measurements. (b) Frequency-resolved error analysis displaying phase deviations (degrees) and modulus differences (percent) at each measured frequency. (c) Experimental and theoretical comparison of impedance modulus and phase for the first model cell including the contribution of the electrodes, Z_{el} , over the 100 Hz–10 MHz frequency range. Data are presented as mean \pm SD from three independent measurements. (d) Frequency-resolved error analysis displaying phase deviations (degrees) and modulus differences (percent) for the electrode-included impedance at each measured frequency.

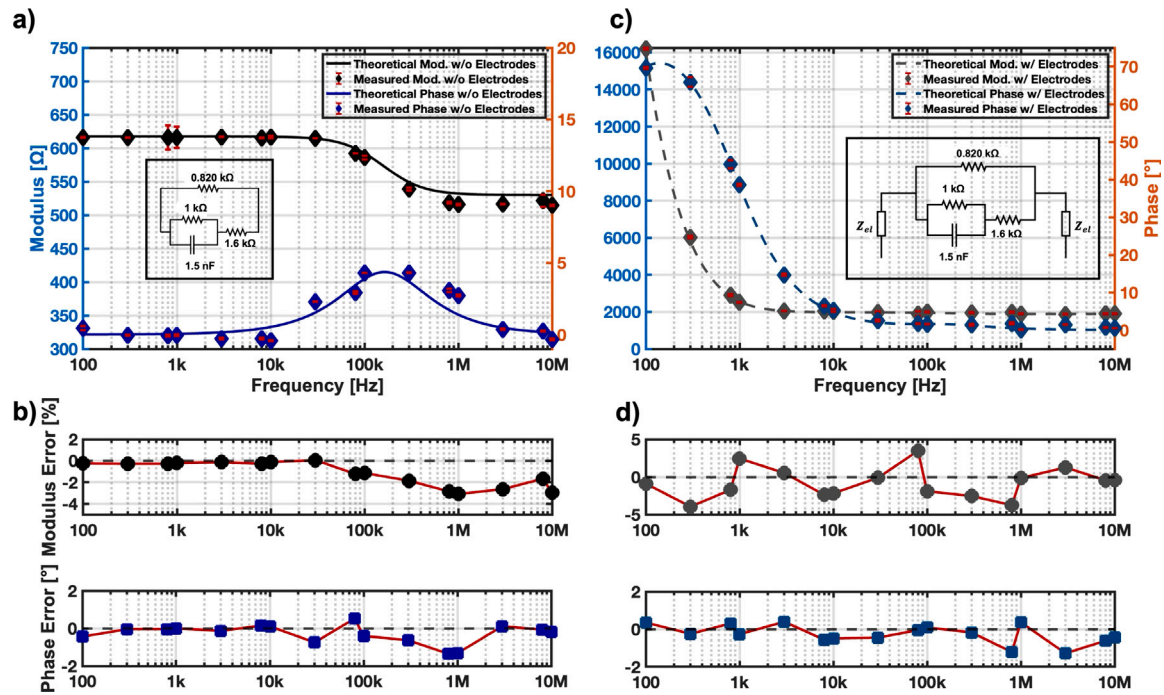


Fig. 6. (a) Experimental and theoretical comparison of impedance modulus and phase for a breast cancer cell model over the 100 Hz–10 MHz frequency range. Data represent the mean \pm SD from three independent experiments. (b) Frequency-resolved error analysis showing phase differences (degrees) and modulus deviations (percent) at each measured frequency. (c) Experimental and theoretical comparison of impedance modulus and phase for a breast cancer cell model including the contribution of the electrodes, Z_{el} , over the 100 Hz–10 MHz frequency range. Data represent the mean \pm SD from three independent experiments. (d) Frequency-resolved error analysis showing phase differences (degrees) and modulus deviations (percent) for the electrode-included impedance at each measured frequency.

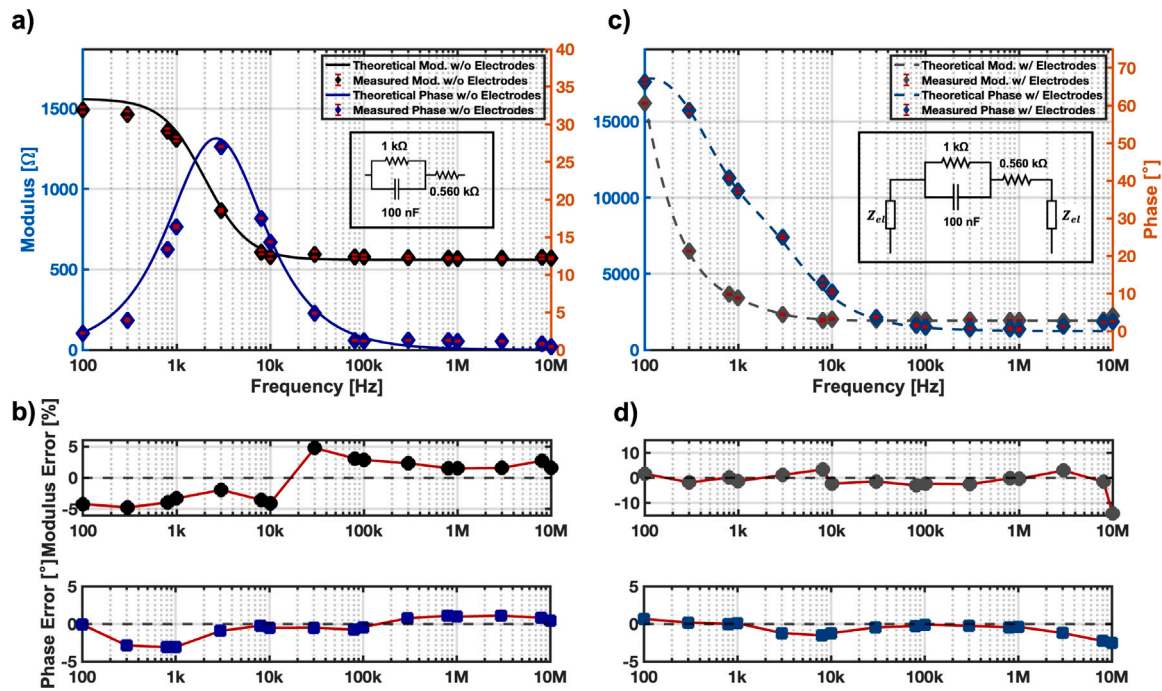


Fig. 7. (a) Experimental and theoretical comparison of impedance modulus and phase for a Cole–Cole model of biceps tissue across the 100 Hz–10 MHz frequency range. Data are presented as mean \pm SD from three independent measurements. (b) Frequency-dependent error analysis showing phase deviations (degrees) and modulus differences (percent) for each frequency point. (c) Experimental and theoretical comparison of impedance modulus and phase for a Cole–Cole model of biceps tissue including the contribution of the electrodes, Z_{el} , across the 100 Hz–10 MHz frequency range. Data are presented as mean \pm SD from three independent measurements. (d) Frequency-dependent error analysis showing phase deviations (degrees) and modulus differences (percent) for the electrode-included impedance at each measured frequency.

allows the developed circuit to address both low-frequency and high-frequency bioimpedance measurements. As shown in Table 1, compared to commercial IC-based solutions, the achieved frequency span is one order of modulus higher (about 10 \times wider) while maintaining reduced estimation errors for both modulus and phase.

Previous works, such as the BIS device developed by [26], demonstrated gain–phase detection using the AD8302 IC but exhibited significant limitations at both low frequencies (below 20 kHz) and high frequencies (above 1 MHz), with validation on RC test circuits. Additional AD8302-based studies [23–25] have further highlighted challenges related to low-frequency accuracy, dynamic-range constraints, and bandwidth limitations. In particular, [23] applied the AD8302 to discriminate different types of meat but operated within a restricted spectral range limited to approximately 100 kHz; [24] characterized mixtures of mineral water and milk across 100 Hz–100 kHz, likewise constrained to the low-frequency regime; and [25] performed measurements on RC test impedances designed to emulate basic bioimpedance behaviors, covering a frequency span from 10 kHz to 125 kHz. In contrast, this work broadens the frequency range to 100 Hz–10 MHz, extending both the lower limit and the conventional upper limit near 1 MHz by one decade, while maintaining high accuracy. This is enabled by an adaptive dynamic-gain and a matched reference path that prevent over-range at the AD8302 inputs and actively compensate inter-path mismatches, preserving linear scaling and reducing systematic errors across the entire bandwidth.

4. Conclusion

We present an impedance-measurement circuit based on the AD8302 IC, supporting a high-frequency range up to 10 MHz. The IC architecture enables linear response characteristics for input signals varying up to ± 20 dB. The proposed measurement approach integrates a feedback gain control mechanism and a reference path to maintain linearity across an extended impedance range, effectively compensating for

phase shifts and amplitude errors introduced by GBW limitations, depending on the ratio between R_{set} and the unknown impedance Z_m . The circuit strategically employs a unity-gain IA not for amplification, but to decouple the current path from the voltage measurement path in both 2- and 4-electrode configurations. Experimental validation demonstrates high measurement accuracy, achieving impedance measurements up to 10 MHz with a maximum modulus error of 14.46% and a maximum phase error of 5.73 $^\circ$. Modulus accuracy can be further improved through compensation methods, while phase resolution for small shifts may benefit from advanced phase detection architectures beyond the multiplier-based implementation of the AD8302. Compared to previous works (Table 1), the proposed design extends the measurable impedance range by one decade, representing a notable improvement in precision and versatility. Future work will include validation of the proposed electronic interface circuit on biological tissues. These investigations will offer a more thorough assessment of the system’s accuracy and robustness under realistic conditions.

CRediT authorship contribution statement

Davide Ciarrocchi: Writing – original draft, Methodology, Investigation, Formal analysis, Conceptualization. **Alessandro Zompanti:** Writing – review & editing, Validation, Supervision. **Marco Santonic:** Writing – review & editing, Validation, Supervision. **Giorgio Pennazza:** Writing – review & editing, Validation, Supervision, Project administration.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Data availability

Data will be made available on request.

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